AMENDMENTS TO THE CLAIMS:

Please amend claims 1-6, 8-12, and 14-16, as indicated below. This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A semiconductor device, comprising:

a wiring board;

a semiconductor chip provided on said wiring board and having a pad electrically connected to a wiring on said wiring board; and

a second semiconductor chip, provided on said wiring board ~~at a position facing a side of said semiconductor chip~~, having a semiconductor substrate with a side facing a side of said semiconductor chip, having a plurality of passive elements integrated ~~therein~~ on said semiconductor substrate, and having a plurality of pads for external connection to which both ends of each of said plurality of [[the]] passive elements are electrically connected respectively, [[and]] at least one of ~~which is~~ said both ends of at least one of said plurality of passive elements is electrically connected via at least one of said plurality of pads for external connection to [[the]] said wiring on said wiring board electrically connected to [[the]] said pad of said semiconductor chip.

2. (Currently Amended) A semiconductor device as set forth in claim 1, wherein [[the]] said plurality of passive elements integrated ~~in said second semiconductor chip~~ on said semiconductor substrate are elements of one kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor.

3. (Currently Amended) A semiconductor device as set forth in claim 1, wherein said semiconductor chip is flipchip-connected to said wiring board so as to electrically connect [[the]] said pad thereof to [[the]] said wiring on said wiring board.

4. (Currently Amended) A semiconductor device as set forth in claim 1, wherein said semiconductor chip has bonding wire connection to [[the]] said wiring of said wiring board so as to electrically connect [[the]] said pad thereof to [[the]] said wiring on said wiring board.

5. (Currently Amended) A semiconductor device as set forth in claim 1, wherein said second semiconductor chip is flipchip-connected to said wiring board ~~so as to electrically connect the pads for external connection to the wiring on said wiring board~~.

6. (Currently Amended) A semiconductor device as set forth in claim 1, wherein said second semiconductor chip has bonding wire connection to [[the]] said wiring of said wiring board ~~so as to electrically connect the pads for external connection to the wiring on said wiring board~~.

7. (Original) A semiconductor device as set forth in claim 1, wherein said semiconductor chip and said second semiconductor chip are both 60 μm or less in thickness.

8. (Currently Amended) A semiconductor device as set forth in claim 5, wherein said second semiconductor chip has~~, besides the~~ at least some of said plurality of pads for external connection used for [[the]] said flipchip connection to said wiring board~~, a pad~~ and at

least some of said plurality of pads for external connection not contributing to [[the]] said flipchip connection to said wiring board.

9. (Currently Amended) A semiconductor device, comprising:

a plurality of semiconductor device portion units arranged in a lamination direction and each including: a wiring board; a semiconductor chip provided on said wiring board; ~~and having~~ a pad electrically connected to a wiring on said wiring board; and a second semiconductor chip, provided on said wiring board ~~at a position facing a side of said semiconductor chip~~, having a semiconductor substrate with a side facing a side of said semiconductor chip, having a plurality of passive elements integrated ~~therein~~ on said semiconductor substrate, and having a plurality of pads for external connection to which both ends of [[the]] each of said plurality of passive elements are electrically connected respectively, [[and]] at least one of ~~which is~~ said both ends of at least one of said plurality of passive elements is electrically connected via at least one of said plurality of pads for external connection to [[the]] said wiring on said wiring board electrically connected to [[the]] said pad of said semiconductor chip; and

a vertical wiring portion passing through said wiring boards of said ~~plural~~ plurality of semiconductor device portion units and electrically connecting said wiring boards to one another.

10. (Currently Amended) A semiconductor device as set forth in claim 9, wherein [[the]] said plurality of passive elements integrated ~~in said second semiconductor chips~~ on said semiconductor substrates of the respective ~~plural~~ plurality of semiconductor device portion units are elements of one kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor.

11. (Currently Amended) A semiconductor package member, comprising:

a wiring board on which a semiconductor chip is mountable; and

an auxiliary semiconductor chip, provided on said wiring board ~~at a position facing a side of said semiconductor chip to be mounted~~, having a semiconductor substrate with a side facing a side of said semiconductor chip to be mounted, having a plurality of passive elements integrated ~~therein~~ on said semiconductor substrate, and having a plurality of pads for external connection to which both ends of [[the]] each of said plurality of passive elements are electrically connected respectively, [[and]] at least one of ~~which is~~ said both ends of at least one of said plurality of passive elements is electrically connected via at least one of said plurality of pads for external connection to a wiring on said wiring board.

12. (Currently Amended) A semiconductor package member as set forth in claim 11, wherein [[the]] said plurality of passive elements integrated ~~in said auxiliary semiconductor chips~~ on said semiconductor substrate are elements of one kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor.

13. (Canceled)

14. (Currently Amended) A semiconductor device as set forth in claim 1, wherein ~~each of the pads of said second semiconductor chip electrically connected to the pad of said semiconductor chip~~ via [[the]] said wiring on said wiring board said at least one of said plurality of pads for external connection of said at least one of said both ends of said at least one of said plurality of passive elements is positioned to be adjacent to said pad of said semiconductor chip.

15. (Currently Amended) A semiconductor device as set forth in claim 9, wherein in each of [[the]] said plurality of semiconductor device portion units, ~~each of the pads of said second semiconductor chip electrically connected to the pad of said semiconductor chip~~ via [[the]] said wiring on said wiring board, said at least one of said plurality of pads for external connection of said at least one of said both ends of said at least one of said plurality of passive elements is positioned to be adjacent to said pad of said semiconductor chip.

16. (Currently Amended) A semiconductor package member as set forth in claim 11, wherein ~~each of the pads of said auxiliary semiconductor chip electrically connected to the wiring on said wiring board~~ said at least one of said plurality of pads for external connection of said at least one of said both ends of said at least one of said plurality of passive elements is positioned to be adjacent to a pad of said semiconductor chip to be mounted, [[the]] said pad ~~being to be connected~~ for connecting to said wiring on said wiring board.